

Notice of References Cited	Application/Control No. 10/630,465	Applicant(s)/Patent Under Reexamination DESAI, KIRAN R.	
	Examiner Jonathan Barton	Art Unit 2186	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,113,514	05-1992	Albonesi et al.	711/144
*	B	US-2004/0186964	09-2004	Dieffenderfer et al.	711/146
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Method for instruction cache coherence on a processor with disjoint level-2 caches. By Disclosed Anonymously. January 29, 2003 IP.com # - IPCOM000010890D
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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